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| Дијаграм тока  микрооперација | Дијаграм тока  управљачких сигнала | Секвенца управљачких сигнала |
| EXEC  EXEC  0  1 | EXEC  EXEC  0  1 | Step00  br(if notEXEC then step00) |
| 1  2  21  …  case(HALT, RTI, RTS, INTE, INTD, ROL, ROR, DEC, BLEQ, BNVF, BLSSU, BOVF, JEQL, BR, JMP, JSR, LD, ST, SUB, ADD, MUL) | 1  2  21  …  case(HALT, RTI, RTS, INTE, INTD, ROL, ROR, DEC, BLEQ, BNVF, BLSSU, BOVF, JEQL, BR, JMP, JSR, LD, ST, SUB, ADD, MUL) | Step01  br(case(HALT, RTI, RTS, INTE, INTD, ROL, ROR, DEC, BLEQ, BNVF, BLSSU, BOVF, JEQL, BR, JMP, JSR, LD, ST, SUB, ADD, MUL) |
| PSWSTART <= 0  [1] HALT  **INTR** | clPSWSTART  [1] HALT  **INTR** | Step02  clPSWSTART, br step37 |
| SP15..0 <= SP15..0 - 1  [2] RTS | decSP  [2] RTS | Step03  decSP |
| MAR15..0 <= SP15..0  SP15..0 <= SP15..0 - 1 | ldMAR, decSP, mxMAR0, mxMAR1 | Step04  ldMAR, decSP, mxMAR0, mxMAR1 |
| MDR7..0 <= MEM[MAR]  FCBUS  0  1 | ldMDR, rdMEM  FCBUS  0  1 | Step05  ldMDR, rdMEM, br(if notFCBUS then step05) |
| DWL7..0 <= MDR7..0  MAR15..0 <= SP15..0 | ldDWL, ldMAR, mxMAR0, mxMAR1 | Step06  ldDWL, ldMAR, mxMAR0, mxMAR1 |
| MDR7..0 <= MEM[MAR]  FCBUS  0  1 | ldMDR, rdMEM  FCBUS  0  1 | Step07  ldMDR, rdMEM, br(if notFCBUS then Step 07) |
| DWH7..0 <= MDR7..0 | ldDWH | Step08  ldDWH |
| PC15..0 <= DWH7..0DWL7..0  **INTR** | ldPC, mxPC1  **INTR** | Step09  ldPC, mxPC1, br step37 |
| SP15..0 <= SP15..0 - 1  [3] RTI | decSP  [3] RTI | Step0A  decSP |
| MAR15..0 <= SP15..0 | ldMAR, mxMAR0, mxMAR1 | Step0B  ldMAR, mxMAR0, mxMAR1 |
| MDR7..0 <= MEM[MAR]  FCBUS  0  1 | ldMDR, rdMEM  FCBUS  0  1 | Step0C  ldMDR, rdMEM, br(if notFCBUS then step 0C) |
| PSW7..0 <= MDR7..0  **[2] RTS** | ldN, ldV, ldZ, ldC, ldI, ldSTART  **[2] RTS** | Step0D  ldN, ldV, ldZ, ldC, ldI, ldSTART, br step03 |
| PSWI <= 1  [4] INTE  **INTR** | stI  [4] INTE  **INTR** | Step0E  stI, br step37 |
| PSWI <= 0  [5] INTD  **INTR** | clI  [5] INTD  **INTR** | Step0F  clI, br step37 |
| A15..0 <= A14..0A15  [6] ROL | slA  [6] ROL | Step10  slA |
| PSWN <= N, PSWZ <= Z  **INTR** | PSWN <= N, PSWZ <= Z  **INTR** | Step11  ldN, ldZ, br step37 |
| A15..0 <= A0A15..1  [7] ROR | srA  [7] ROR | Step12  srA |
| PSWN <= N, PSWZ <= Z  **INTR** | PSWN <= N, PSWZ <= Z  **INTR** | Step13  ldN, ldZ, br step37 |
| A15..0 <= A15..0 – 1,  PSWC <= C, PSWV <= V  [8] DEC | sub, mxALU, ldA,  ldC, ldV  [8] DEC | Step14  sub, mxALU, ldA, ldC, ldV |
| PSWN <= N, PSWZ <= Z  **INTR** | ldN, ldZ  **INTR** | Step15  ldN, ldZ, br step37 |
| (N ^ V) + Z  [9] BLEQ  0  1 | (N ^ V) + Z  [9] BLEQ  0  1 | Step16  br(if notsignal1 then step37) |
| PC15..0 <= PC15..0 + IR23..IR23..16  **INTR** | ldPC,  mxPC0  **INTR** | Step17  ldPC, mxPC0, br step37 |
| V  [10] BNVF  1  0 | V  [10] BNVF  1  0 | Step18  br(if V then step37) |
| PC15..0 <= PC15..0 + IR23..IR23..16  **INTR** | ldPC,  mxPC0  **INTR** | Step19  ldPC, mxPC0, br step37 |
| C  [11] BLSSU  0  1 | C  [11] BLSSU  0  1 | Step1A  br(if notC then step37) |
| PC15..0 <= PC15..0 + IR23..IR23..16  **INTR** | ldPC,  mxPC0  **INTR** | Step1B  ldPC, mxPC0, br step37 |
| V  [12] BOVF  0  1 | V  [12] BOVF  0  1 | Step1C  br(if notV then step37) |
| PC15..0 <= PC15..0 + IR23..IR23..16  **INTR** | ldPC,  mxPC0  **INTR** | Step1D  ldPC, mxPC0, br step37 |
| Z  [13] JEQL  0  1 | Z  [13] JEQL  0  1 | Step1E  br(if notZ then step37) |
| PC15..0 <= IR23..8  **INTR** | ldPC  **INTR** | Step1F  ldPC, br step37 |
| [14] BR  PC15..0 <= PC15..0 + IR23..IR23..16  **INTR** | [14] BR  ldPC,  mxPC0  **INTR** | Step20  ldPC, mxPC0, br step37 |
| [15] JMP  PC15..0 <= IR23..8  **INTR** | [15] JMP  ldPC  **INTR** | Step21  ldPC, br step37 |
| MAR15..0 <= SP15..0  MDR7..0 <= PC15..8  SP15..0 <= SP15..0 + 1  [16] JSR | ldMAR, mxMAR1, mxMAR0, ldMDR, mxMDR1, incSP  [16] JSR | Step22  ldMAR, mxMAR1, mxMAR0, ldMDR, mxMDR1, incSP |
| MEM[MAR] <= MDR7..0  FCBUS  0  1 | wrMEM  FCBUS  0  1 | Step23  wrMEM, br(if notFCBUS then step23) |
| MAR15..0 <= SP15..0  MDR7..0 <= PC7..0  SP15..0 <= SP15..0 + 1 | ldMAR, mxMAR1, mxMAR0, ldMDR, mxMDR1, mxMDR0, incSP | Step24  ldMAR, mxMAR1, mxMAR0, ldMDR, mxMDR1, mxMDR0, incSP |
| MEM[MAR] <= MDR7..0  FCBUS  0  1 | wrMEM  FCBUS  0  1 | Step25  wrMEM, br(if notFCBUS then step25) |
| PC15..0 <= IR23..8  **INTR** | ldPC  **INTR** | Step26  ldPC, br step37 |
| A15..0 <= B15..0  [17] LD | ldA  [17] LD | Step27  ldA |
| PSWN <= N, PSWZ <= Z  **INTR** | ldN, ldZ  **INTR** | Step28  ldN, ldZ, br step37 |
| immed  [18] ST  1  0 | immed  [18] ST  1  0 | Step29  br(if immed then step37) |
| regdir  1  0 | regdir  1  0 | Step2A  br(if regdir then step30) |
| MDR7..0 <= A15..8 | ldMDR, mxMDR2, mxMDR0 | Step2B  ldMDR, mxMDR2, mxMDR0 |
| MEM[MAR] <= MDR7..0  FCBUS  0  1 | MEM[MAR] <= MDR7..0  FCBUS  0  1 | Step2C  wrMEM, br(if notFCBUS then step2C) |
| MAR15..0 <= MAR15..0 + 1  MDR7..0 <= A7..0 | incMAR, ldMDR, mxMDR0 | Step2D  incMAR, ldMDR, mxMDR0 |
| MEM[MAR] <= MDR7..0  FCBUS  0  1 | MEM[MAR] <= MDR7..0  FCBUS  0  1 | Step2E  wrMEM, br(if notFCBUS then step2E) |
| **INTR** | **INTR** | Step2F  br step37 |
| GPR[IR19..16]15..0 <= A15..0​  **INTR** | wrGPR ​  **INTR** | Step30  wrGPR, br step37 |
| A15..0 <= A15..0 – B15..0  PSWV <= V, PSWC <= C  [19] SUB | ldA, mxA0, sub,  ldV, ldC  [19] SUB | Step31  ldA, mxA0, sub, ldV, ldC |
| PSWN <= N, PSWZ <= Z  **INTR** | ldN, ldZ  **INTR** | Step32  ldN, ldZ, br step37 |
| A15..0 <= A15..0 + B15..0  PSWV <= V, PSWC <= C  [20] ADD | ldA, mxA0, add  ldV, ldC  [20] ADD | Step33  ldA, mxA0, add, ldV, ldC |
| PSWN <= N, PSWZ <= Z  **INTR** | ldN, ldZ  **INTR** | Step34  ldN, ldZ, br step37 |
| A15..0 <= A7..0 \* B7..0  PSWV <= V, PSWC <= C  [21] MUL | ldA, mxA0, mul,  ldV, ldC  [21] MUL | Step35  ldA, mxA0, mul, ldV, ldC |
| PSWN <= N, PSWZ <= Z  **INTR** | ldN, ldZ  **INTR** | Step36  ldN, ldZ |
| EXEC <= 0, INTR <= 1  INTR  **EXEC** | clEXEC, stINTR  INTR  **EXEC** | Step37  clEXEC, stINTR, br step00 |

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